DS1259

Battery Manager Chip

Not Recommended for New Designs

Part Number	Replacement	Explanation
DS1259	n/a	This product is being discontinued and is subject to Last Time Buy, after which new orders can not be placed.
DS1259+	n/a	
DS1259N	n/a	
DS1259S	n/a	
DS1259S+	n/a	
DS1259SN	n/a	
DS1259SN+	n/a	

Description

The DS1259 Battery Manager Chip is a low-cost battery management system for portable and nonvolatile electronic equipment. A battery connected to the battery input pin supplies power to CMOS electronic circuits when primary power is lost through an efficient switch via the V_{CCO} pins. When power is supplied from the battery, the power-fail signal is active to warn electronic reset circuits of the power status. Energy loss during shipping and handling is avoided by pulsing reset, thereby causing the battery to be isolated from other elements in the circuits.

Key Features

- Facilitates uninterruptible power
- Uses battery only when primary V_{CC} is not available
- Low forward voltage drop
- Power fail signal interrupts processor or write protects memory
- Consumes less than 100nA of battery current
- Low battery warning signal
- Battery can be electrically disconnected upon command
- Battery will automatically reconnect when V_{CC} is applied
- Mates directly with DS1212 Nonvolatile Controller x 16 Chip to back up 16 RAMs
- Optional 16-pin SOIC surface-mount package
- Underwriters Laboratories (UL®) Recognized

Evaluation Kits

Reliability Reports

Reliability Report: DS1259.pdf
Underwriters Laboratories (UL®) Recognized

Software/Models

Ordering Information

Devices: 1-11 of 11

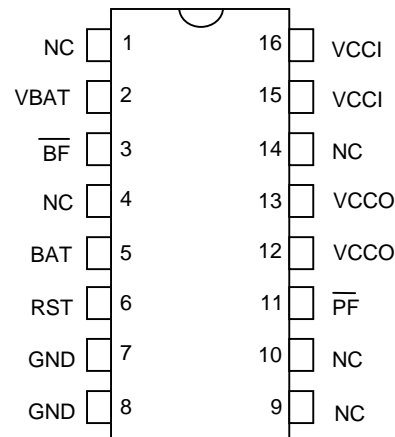| DS1259	Free Sample	Buy	Package: TYPE PINS FOOTPRINT DRAWING CODE/VAR *	Temp	RoHS/Lead-Free? Materials Analysis
DS1259+			PDIP;16 pin; Dwg: 21-0043 (PDF) Use pkgcode/variation: P16+2*	0°C to +70°C	RoHS/Lead-Free: Lead Free Materials Analysis
DS1259			PDIP;16 pin; Dwg: 21-0043 (PDF) Use pkgcode/variation: P16-2*	0°C to +70°C	RoHS/Lead-Free: No Materials Analysis
DS1259N			PDIP;16 pin; Dwg: 21-0043 (PDF) Use pkgcode/variation: P16-2*	-40°C to +85°C	RoHS/Lead-Free: No Materials Analysis
DS1259S+T&R			SOIC;16 pin; Dwg: 21-0042 (PDF) Use pkgcode/variation: W16+3*	0°C to +70°C	RoHS/Lead-Free: Lead Free Materials Analysis
DS1259SN+			SOIC;16 pin; Dwg: 21-0042 (PDF) Use pkgcode/variation: W16+11*	-40°C to +85°C	RoHS/Lead-Free: Lead Free Materials Analysis
DS1259SN+T&R			SOIC;16 pin; Dwg: 21-0042 (PDF) Use pkgcode/variation: W16+11*	-40°C to +85°C	RoHS/Lead-Free: Lead Free Materials Analysis
DS1259S			SOIC;16 pin; Dwg: 21-0042 (PDF) Use pkgcode/variation: W16-11*	0°C to +70°C	RoHS/Lead-Free: No Materials Analysis
DS1259S+			SOIC;16 pin; Dwg: 21-0042 (PDF) Use pkgcode/variation: W16+11*	0°C to +70°C	RoHS/Lead-Free: Lead Free Materials Analysis
DS1259S/T&R			SOIC;16 pin; Dwg: 21-0042 (PDF) Use pkgcode/variation: W16-11*	0°C to +70°C	RoHS/Lead-Free: No Materials Analysis
DS1259SN			SOIC;16 pin; Dwg: 21-0042 (PDF) Use pkgcode/variation: W16-11*	-40°C to +85°C	RoHS/Lead-Free: No Materials Analysis
DS1259SN/T&R			SOIC;16 pin; Dwg: 21-0042 (PDF) Use pkgcode/variation: W16-11*	-40°C to +85°C	RoHS/Lead-Free: No Materials Analysis

FEATURES

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- Power fail signal interrupts processor or write protects memory
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- Mates directly with DS1212 Nonvolatile Controller x 16 Chip to back up 16 RAMs
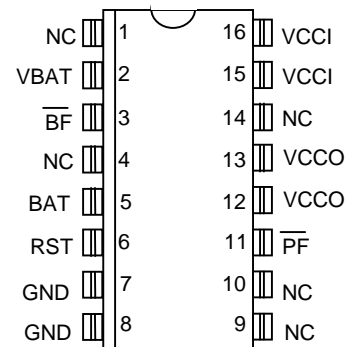- Optional 16-pin SOIC surface-mount package

PIN DESCRIPTION

NC	- No Connect
V_{BAT}	- Battery Input Connection
$\overline{BF}$	- Battery Fail Output Signal
BAT	- Battery Output
RST	- Reset Input
GND	- Ground
$\overline{PF}$	- Power Fail Output Signal
V_{CCO}	- RAM Supply
V_{CCI}	- +5V Supply

PIN ASSIGNMENT

NC	1	16	VCCI
VBAT	2	15	VCCI
$\overline{BF}$	3	14	NC
NC	4	13	VCCO
BAT	5	12	VCCO
RST	6	11	$\overline{PF}$
GND	7	10	NC
GND	8	9	NC

16-Pin DIP Package (300-mil)
See Mech. Drawings Section

NC	1	16	VCCI
VBAT	2	15	VCCI
$\overline{BF}$	3	14	NC
NC	4	13	VCCO
BAT	5	12	VCCO
RST	6	11	$\overline{PF}$
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16-Pin SOIC Package (300-mil)
See Mech. Drawings Section

DESCRIPTION

The DS1259 Battery Manager Chip is a low-cost battery management system for portable and nonvolatile electronic equipment. A battery connected to the battery input pin supplies power to CMOS electronic circuits when primary power is lost through an efficient switch via the V_{CCO} pins. When power is supplied from the battery, the power-fail signal is active to warn electronic reset circuits of the power status. Energy loss during shipping and handling is avoided by pulsing reset, thereby causing the battery to be isolated from other elements in the circuits.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground   -0.3V to +7.0V
Operating Temperature   0°C to 70°C
Storage Temperature   -55°C to +125°C
Soldering Temperature   260°C for 10 seconds

*   This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS   (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Primary Power Supply	V_{CCI}		5	5.5	V	1
Input High Voltage	V_{IH}	2.0		V_{CC}+0.3	V	1
Input Low Voltage	V_{IL}	-0.3		+0.8	V	1
Battery Voltage Pin 2	V_{BAT}	2.5	3	3.7	V	6
Battery Output Pin 5	BAT	V_{BAT}-0.1			V	1

DC ELECTRICAL CHARACTERISTICS   (0°C to 70°C; V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Leakage Current	I_{LO}	-1.0		+250	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	1, 2
Output Current @ 0.4V	I_{OL}			+4.0	mA	1, 2
Input Supply Current	I_{CCI}			10	mA	3
Pins 12, 13 $V_{CCO}=V_{CCI}$-0.2	I_{CCO}			250	mA	
Pin 11 $\overline{PF}$ Detect	V_{TP}	(1.26xV_{BAT}) -250mV	(1.26xV_{BAT}) +250mV		V	4, 6
Pin 3 $\overline{BF}$ Detect	V_{BATF}	1.5	2.0	2.6	V	7

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pins 12, 13 $V_{CCO}=V_{BAT}$-0.2V	I_{CCO2}			15	mA	5
Battery Leakage	I_{BAT}			100	nA	8
Pin 5 Battery Output Current	I_{BATOUT}			100	µA	

CAPACITANCE   (T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Output Capacitance	C_{OUT}		5	10	pF	

AC ELECTRICAL CHARACTERISTICS   (0°C to 70°C; V_{CC} = 4.0 to 5.5V)

| PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CCI} Slew Rate	t_F	300			µs	
V_{CCI} Slew Rate	t_R	1			µs	
Power-Down to $\overline{PF}$ Low	t_{PF}	0			µs	
$\overline{PF}$ High after Power-Up	t_{REC}			100	µs	9

# POWER-DOWN/POWER-UP CONDITION
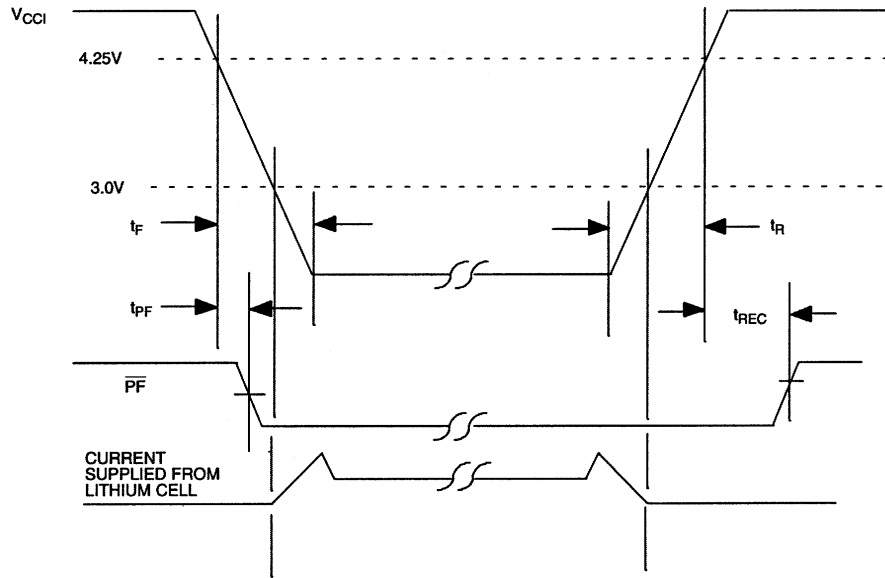
NOTES:

1. All voltages are referenced to ground.

2. Load capacity is 50 pF.

3. Measured with Pins 11, 12, 13, and 3 open.

4. V_{TP} is the point that $\overline{PF}$ is driven low.

5. I_{CCO2} may be limited by the capability of the battery.

6. Trip point voltage for power-fail detect:
    $V_{TP} = 1.26 \times V_{BAT} \pm 250$ mV
    For 5% operation: $V_{BAT} = 3.7V$ max.
    For 10% operation: $V_{BAT} = 3.5V$ max.

7. V_{BATF} is the point that $\overline{BF}$ is driven low. These limits are for 0°C to 70°C operation.

8. Battery leakage is the internal energy consumed by the DS1259.

9. $V_{CC} = +5$ volts, $t_A = 25$°C.

N
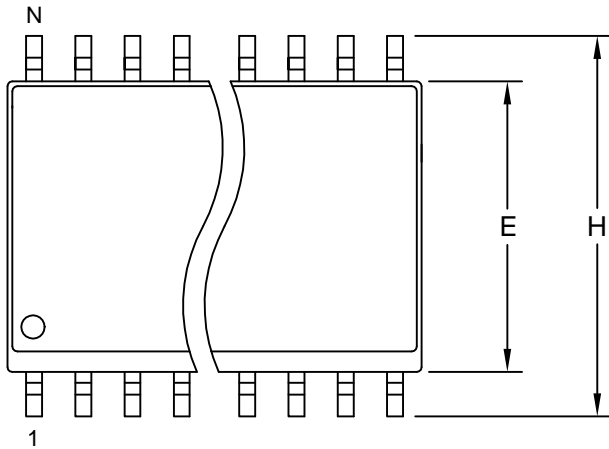
TOP VIEW
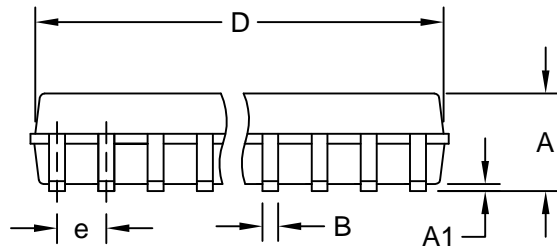
FRONT VIEW

SIDE VIEW

0°-8°
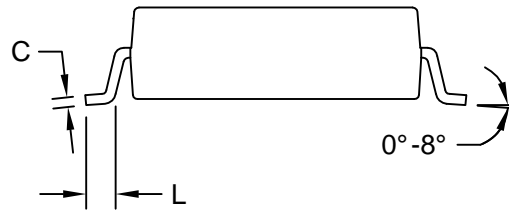
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
e	0.050		1.27	
E	0.291	0.299	7.40	7.60
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27

VARIATIONS:

	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS013
D	0.398	0.413	10.10	10.50	16	AA
D	0.447	0.463	11.35	11.75	18	AB
D	0.496	0.512	12.60	13.00	20	AC
D	0.598	0.614	15.20	15.60	24	AD
D	0.697	0.713	17.70	18.10	28	AE

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS013.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR **MAXIM**

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, .300" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	1/1
	21-0042	B	